PXIE LEBT EXTRACTION ELECTRODE MODULATOR MANUAL

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1 INTRODUCTION

The following document describes the design requirements, interface to the Modulator's control and some design details. This Modulator is a modified version of the LEBT Chopper Driver. This modulator is a "quick" design to test the feasibility of gating/pulsing beam from the H- source that is designed to operate CW.

This modulator accepts the output of the Extraction Electrode HV DC PS (EEPS) as an input. It contains a HV bipolar switch that either outputs the EEPS voltage or zero volts—local common (the isolated -30 kV). The design of this modulator, including the control as well as the hardware, is based off the original design of the PXIE LEBT Chopper Driver; which was itself a modified version of the Electron Cooling Gun Modulator as an attempt to put something together with the least amount of work.

This Modulator will initially be controllable via a LabView application running on a PC. Control and interface via ACNET can be provided by outfitting any ACNET frontend node with the appropriate protocol to communicate with the modulator. The preferred way to do this is for the frontend to use the same protocol used by the LabView application. The necessary information to do this is described in section 3 Ethernet Communication.

1.1 Specifications

Table 1.1 lists the Modulator's design parameters.

Table 1.1. Extraction Electrode Modulator requirements.

Parameter	**Description**	**Value**
Pulse length	> 90% of maximum intensity	1-16,665 μsec
Rise/fall time	10% - 90%	~0.2 μsec
Pulse repetition rate	In either externally triggered or free-running modes	1 - 60 Hz
Output voltage	DC coupled, defined by Extraction Electrode HV DC PS	5 kV
Electrode capacitance	Sum of capacitance to earth ground and plasma electrode	~220 pF
Input / output low level signals		
Trigger input	Mode 2 operation only. Rising edge triggers beam output.	TTL, 50 Ohm internally terminated
Beam Sync output	A pulse coincident with beam generated. Routed to Controls Clock Generator at ground level.	Fiber optic cable, Versalink termination
nReady output	Indication that all fault status bits are cleared and the Modulator is ready to output beam	Closed contact

1.2 Modulator Operational Features

This section describes the basic Driver operating features. Interface control, at least initially, will be by way of a LabView application that is described in section 2.1.

All references to a "trip" are events resulting in the Modulator advancing to Mode 0. The event causing the trip will indicate among the latched Status bits listed in Table 3.4, assuming the condition is one of those items identified. For example, who knows what will happen when the H- Source sparks?

1.2.1 Modulator "Ready" state

Certain conditions must be met for the Modulator to allow beam. If the Modulator is in a condition to allow beam it is said to be "Ready". The Ready condition depends on summation of the following parameters:

A. The Behlke high voltage switch is not faulted.
B. Pulse width does not exceed the pulse period.

Note that each of these fault conditions is latched. Thus, the user will always have the ability to determine the reason for a trip, even if the fault was momentary. The user must clear fault indications by issuing a control bit "Reset" in order to run.

The following explains the system status listed in Table 3.4. Note that two status bits are grayed-out in the table that pertain only to the Chopper Driver and not the Extraction Electrode Modulator.

Chassis Ready — This condition is a summation of parameters A and B above. The Ready condition is brought out on a chassis connector intended to be routed to Controls; see Table 1.2.

Behlke OK — The internal commercial switch has a read back fault status bit and is monitored and included in the Ready summation chain.

Pulse Width OK — This indicates a fault if the pulse width is chosen to be wider than the pulse period. This detection is applied in both modes 2 and 3. Pulsing will stop, since the Ready condition will trip and the mode will advance to mode 0. To prevent this trip from occurring again, the user must change either the pulse width or rep rate.

1.2.2 Operating modes

The Modulator has five operational modes. The Modulator state of readiness, as described above, as well as user choices determine the operational mode. The mode is an analog setting parameter.

Mode 0: This mode is entered automatically whenever the Modulator's operating condition is not Ready. In this mode, the output is zero volts. Monitoring system status will indicate the cause for not being Ready. Issuing a Reset will clear all fault indications, provided the fault condition has cleared. Should the fault be cleared and the user issues a reset, then the mode will advance to 1. Note that the mode will not automatically advance to Mode 1 if a fault condition goes away on its own.

Mode 1: The Modulator enters Mode 1 when all fault conditions have cleared and the user has issued a Reset. In this mode the chassis will be in the Ready, and the Modulator output remains zero volts. The user must set the operating mode to 2, 3 or 4 to output beam. Selecting Mode 1 when in 2, 3 or 4 shuts beam off.

Mode 2: The Modulator responds to external TCLK triggers in this mode. Allowable external trigger rates are anything up to and including 60 Hz. While the pulse period is determined by the External triggers, the pulse width is determined by the user's entry of the pulse width setting value. Should the pulse width be set wider than the input trigger's period, the Driver will stop pulsing and enter Mode 0. Monitoring the status will reveal this trip condition. The user must rectify the situation and Reset the Driver before returning to Mode 2.

Also, it is in this mode that the user can issue one-shot triggers by way of actuating control bit 1. Refer to Table 3.5.

Mode 3: This is the free-running pulse mode. The pulse rate is set as an analog setting parameter in the range of 1 to 60 Hz, inclusive.

Mode 4: DC operating mode.

The user is free to change operating modes between 1, 2, 3 and 4 at will. Also, the pulse width and pulsing rep rate can be changed at any time.

1.3 Chassis I/O Connections

Table 1.2 lists the chassis input and output connections other than 120 VAC power connector.

Table 1.2. Chassis signal connectors.

Signal	Input or output	Description
Ethernet	In & out	RJ-45 connector. A media converter box accompanies this Modulator.
HV DC In	Input	SHV connector. Input from Extraction Electrode HV DC PS
HV Out	Output	SHV connector. Output to Extraction Electrode
Trigger	Input	BNC, 50 Ohm terminated, TTL. A rising edge triggers a pulse of beam.
Beam Sync	Output	Fiber-optic, Versalink. Routed to Controls Clock Generator at ground level where a media converter module converts this to an electric signal.
nReady	Output	Contact closer indicates a "ready" condition on a twinax connector. It is a summation of conditions. The contact current limit is about 10 mA having a voltage drop of 1.2 V.

1.4 Front Panel LED Indications

Table 1.3. Front panel LED indications.

LED	Indication
1	Heart beat, blinks at 1/2 Hz
2	Modulator Ready
3	Ethernet error in reception
4	Ethernet communication received
5	Mode 2
6	Mode 3
7	Mode 4
8	n/a

2 MODULATOR CONTROL

2.1 Using The LabView Application RabbitUI For Control

Control of the Extraction Electrode Modulator is by way of the RabbitUI LabView application. This program interfaces to a number of accelerator systems. Therefore, the first thing the user needs to do upon starting this application is choose to control the Extraction Electrode Modulator. To do this click on the drop-down box under "Rabbit System Hostname" and select "LEBTExtnEl.fnal.gov" from the list.

This LabView application's interface design is taken from ACNET philosophy. The Modulator has readings, settings, status and control data associated with its control. Data is arranged into four arrays for the purpose of communication between a network "client", in this case the LabView application or an ACNET parameter page, and the Modulator chassis acting as a network "server". Settings can be both sent to the Modulator and read back, so this brings the count to five possible "actions" corresponding to the five tabs on the interface. Some explanation of the control functions on these five tabs is in order.

Read — There are two readings, namely, the voltage of the high voltage power supply in the Driver and the output voltage. (These two voltages had better be the same when beam is cut off or something is wrong.) These two readings are listed in Table 3.2.

Read setting — Settings values can be read back. This action must be chosen by depressing the button. The readable settings are the same as the list of settable parameters listed in Table 3.3.

Read status — Status bits are read back. There are labels identifying each status bit. Furthermore, status is arranged in groups of 16 digital words in the case of systems having a lot of status. Also, similar to the pull-down boxes in "Read setting", pull-down boxes provide the means to select a limited range of all status bits available within each word. The status bits are listed in Table 3.4.

Set a setting — Settable parameters are controlled one at a time. Thus, select the desired parameter from the "Element" list. This tab provides the ability to enter either a scaled or raw (unscaled 16-bit integer) value. Enter a value in one of the two text boxes and then click the corresponding blue button. The blue box "Read Current Values" provides the means to read back what is now in the chosen element. Settings are listed in Table 3.3.

Set a control bit — Control bits are also arranged in an array of 16-bit words. The "Element" list is used to select the desired word of bits. (Typically there aren't many control bits in an application.) Only one control bit <u>must</u> be set at a time. Select only one bit to be on and click "Set a control bit". Control bits are listed in Table 3.5.

3 ETHERNET COMMUNICATION

The Chopper Driver is controlled is by way of a LabView application over Ethernet. The network parameters for communicating with the Driver chassis are given in Table 3.1.

Table 3.1. Driver chassis network parameters.

Network parameter	Value
Device Name	LEBTExtnEl
IP Address	131.225.142.137
VLAN	?
Local Port	4524
Network Mask	255.255.255.0
Gateway	131.225.142.200

3.1 Ethernet Client/Server Communication Data Structures

The convention for communication between the Modulator chassis and the LabView application is by implementing the protocol spelled out in the document *The Compact Ethernet Communication (CEC) Protocol*, Beams-doc_2109-v1. In conformance with this protocol, four data arrays are defined and shown in Tables 2.2 through 2.5.

The Rabbit RCM services requests over Ethernet and is therefore a server. The network device making requests will be referred to in the rest of this document as the "client".

Analog scale factors are shown in the Analog Range column. The analog binary codes are 16-bit unsigned, unipolar for the ADC and DAC values.

Table 3.2. Array of analog readings. Used for Message Type Code 0.

Element No.	ACNET Parameter	Device Description	Displayed Units	Analog Range 0x0000 - 0xFFFF
0	n/a	Extraction electrode PS voltage	kVdc	0 – 5
1	n/a	Output voltage	kVdc	0 – 5

Table 3.3. Array of analog settings. Used for Message Type Codes 1 & 3.

Element No.	ACNET Parameter	Device Description	Displayed Units	Analog Range 0x0000 - 0xFFFF
0	n/a	Operating mode number. Valid modes are: 0,1, 2, 3 or 4	none	Mode is integer value
1	n/a	Beam pulse width (Value 0 is not accepted.)	µs	0 – 16,665 as an integer value in the range
2	n/a	Free running pulse frequency. Mode 3 operation only. (Value 0 is not accepted.)	Hz	1 - 60 as an integer value in the range

Table 3.4. Array of status. Used for Message Type Code 2.

Element Number	Data Bit	Device	ACNET Parameter
0	0	Modulator Ready (1 = True, 0 = False)	n/a
	1	Behlke switch is not faulted (1 = OK, 0 = Fault)	n/a
	2	Pulse width is OK, i.e. pulse width is less than pulse period (1 = OK, 0 = Error)	n/a

Table 3.5. Array of control. Used for Message Type Code 4. A bit set to 1 performs the function. Only one bit can be/should be set per command.

Element Number	Data Bit	Device	ACNET Parameter
0	0	Reset (1 = reset)	n/a
	1	Manual Trigger, in mode 2 only (1 = trigger)	n/a
	2	Interrupt 1 acknowledge (1 = ack)	n/a

4 CIRCUIT DESCRIPTION

The controller in the Modulator chassis is a three-PCB assembly located in the low voltage section of the chassis. The first board of the three-board controller is a highly configurable digital board referred to as a Modular Ethernet Configurable Controller (MECC) board. Its two major components are a commercial 8-bit computer on a sub-credit card size PCB and a complex programmable logic device (CPLD) IC. The computer board is a Rabbit Core Module (RCM) model RCM3010 with Ethernet capability. The CPLD is an Altera EPM1270. The second board of the assembly is a data acquisition board with 16 channels of 16-bit ADC and 4 channels of 14-bit DAC. The third board interfaces with the HV DC PS in the chassis.

4.1 Addressing System Devices

This section documents a convention employed on the digital controller board for communication between the computer RCM and the CPLD. The design of this module is a trimmed down version of the E-Cool Gun Modulator, so the number of internal parameters controlled is very few. None the less, it is necessary to understand the communication protocol used between the RCM and CPLD.

The Modulator contains circuitry that needs to be controlled. Every "item" controlled is considered a "device", and all devices are under the control of the RCM by way of logic in the CPLD. The RCM reads and writes to defined registers in the CPLD to control each of the specific devices defined in the system. ICs such as a multi-channel A/D and D/A converters are each a device. Also, things such as pulse width control and status registers are also defined devices. Each device is assigned a register address, and the RCM reads from and writes to these registers.

The concept of an address and data bus is quite conventional, but it is worth mentioning that using a bus for control with external hardware is an optional RCM feature. Specific C language function calls set up this bus feature for communicating with external hardware. The RCM writes to and/or reads from defined registers in the CPLD for some control of hardware, but not necessarily all. Rabbit documentation refers to the use of its external bus as the "external I/O" and also "auxiliary I/O" bus, depending where you are reading in the documentation. This external I/O bus comprises an 8-bit data bus and a 6-bit address. These lines are shown on the Appendix Fig. A.1 diagram interconnecting the RCM with the CPLD. Also shown are additional I/O lines between the RCM and CPLD. Some of these lines are used and described later.

4.2 Register Definitions and RCM to CPLD Interface signals

Table 4.1 shows the registers defined in the CPLD that the RCM reads and write to. Note that although the RCM external/auxiliary I/O bus only contains 6 bits of address, Table 4.1 Address column shows 32 bits. Per the Rabbit RCM design, writing to the higher address bits sets the strobe type to be used. Strobes are configured as described in Table 4.2. The Table 4.1 Address column correlates with Table 4.2 Address Range. Writing to a specific address range defines which strobe will be issued.

Also, several individual general RCM configurable I/O lines are used listed in Table 4.3. Refer to Appendix Tables A.2 and A.3 as a reference for the RCM port and pin alternate functions. The spread sheet column C, "Altera Pin", identifies which of the Alter EPM1270 CPLD pins have been interconnected to the RCM's I/O pins in the PCB layout. This spread sheet reveals what is available for any configuration, not for simply the Modulator. Tables 4.1, 4.2 and 4.3 identify what has been committed specifically for the Modulator.

Table 4.1. Device registers defined in the CPLD . The Read/Write indication is with respect to RCM control. All registers are 8 bits. Strobe PE4 is used on all writes, PE5 is used on all reads.

Device Register	Comments		R/W	Address
Operating mode register	Values are 0, 1, 2, 3 or 4		W	0x8001
			R	0xA001
Pulse width, Unit of time is microseconds, Value is a 2-byte word	LS byte		W	0x8002
	MS byte		W	0x8003
Free-running pulse period, Unit of time is microseconds, Value is a 4-byte long word, Used in operating mode 2 only	LS word	LS byte	W	0x8004
		MS byte	W	0x8005
	MS word	LS byte	W	0x8006
		MS byte	W	0x8007
Status register	Status bits as per Table 3.4		R	0xA008
Control register	Status bits as per Table 3.5		W	0x8009

Table 4.2. Strobe configurations. Address range relates to addresses shown in Table 3.1.

Bit	Type	Sense	Wait States	Address Range
PE4	Write	Active HI	1	0x8000 – 0x9FFF
PE5	Read	Active HI	1	0xA000 – 0xBFFF

Table 4.3. RCM general, configurable I/O lines used to interface with the CPLD. Direction of I/O is with respect to the RCM.

Bit	RCM Pin	CPLD Pin	Function	RCM In/Out	
PB0	J2/2	5	SPI clock. Configured for alt. function CLKB	Out	
PC5	J1/20	6	SPI MISO, master in slave out. PC5 is configured for alt. function RxB	In	
PC4	J1/19	7	SPI MOSI, master out slave in. PC5 is configured for alt. function TxB	Out	
PE6	J2/14	3	ADC chip select line	Out	
PE4	J2/16	1	STR4, Strobe 4, RCM write	Out	
PE5	J2/15	2	STR5, Strobe 5, RCM read	Out	
PE1	J2/18	143	Interrupt 1 line, active high (1)	In	

(1) See chapter 7 in the Rabbit 3000 Microprocessor User’s Manual, 019-0108_Z, per external interrupts.

APPENDIX SECTION A.

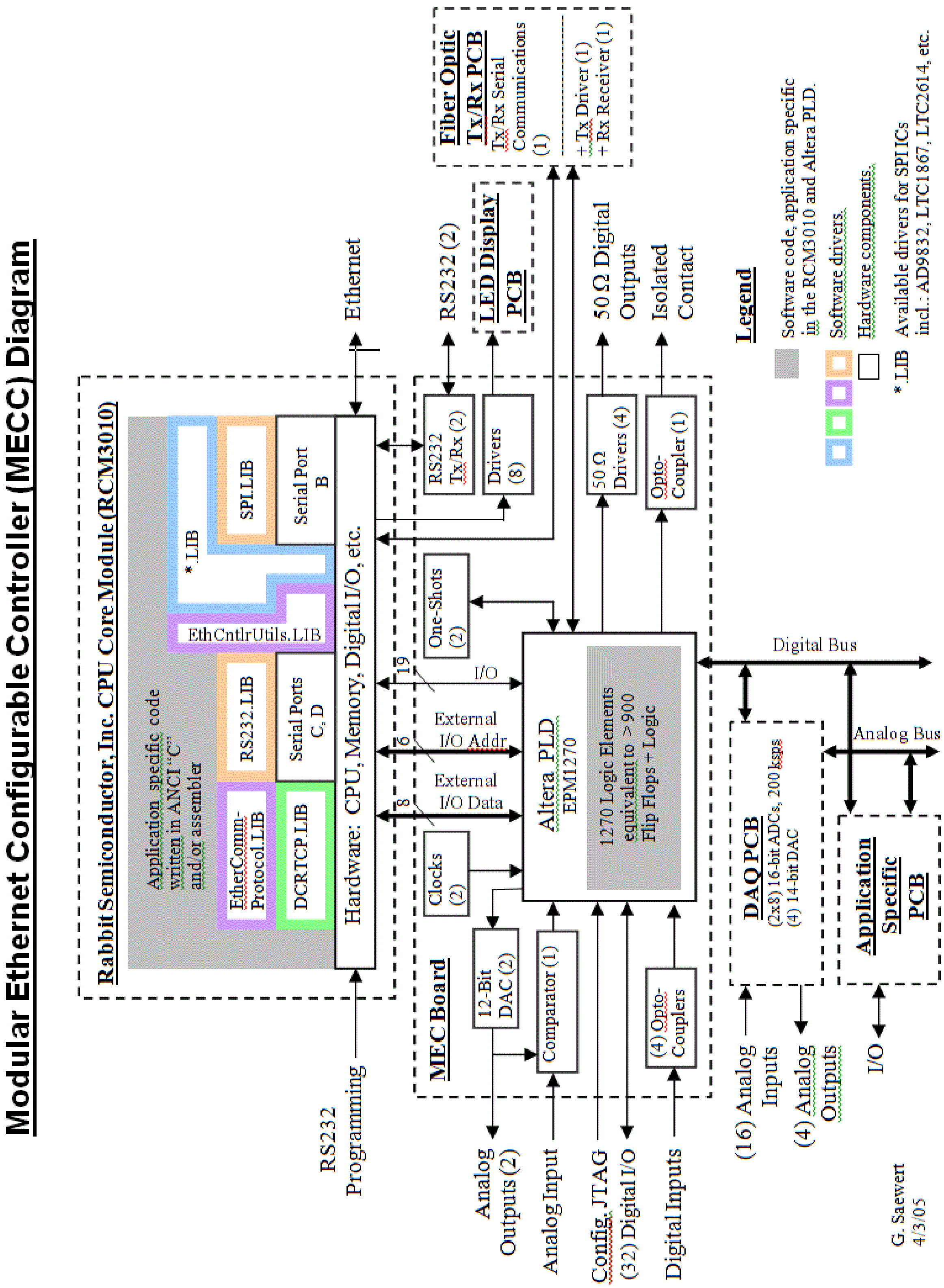

Fig. A.1. Controller assembly block diagram. Refer to the text for a description of those features used in the Chopper Driver Controller.

PARALLEL PORT A

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	PRIMARY FUNCTION DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION I/O	CAPA-BILITY
D7	J1/3	23	PA7	IN	PARALLEL I/O		SD7, ID7	I/O
D6	J1/4	24	PA6	IN			SD6, ID6	I/O
D5	J1/5	27	PA5	IN			SD5, ID5	I/O
D4	J1/6	28	PA4	IN			SD4, ID4	I/O
D3	J1/7	29	PA3	IN			SD3, ID3	I/O
D2	J1/8	30	PA2	IN			SD2, ID2	I/O
D1	J1/9	31	PA1	IN			SD1, ID1	I/O
D0	J1/10	32	PA0	IN			SD0, ID0	I/O

SLAVE PORT
CONTROL REGISTER
SPCR (0x24)

7	0
6	0
5	0
4	0
3, 2	00=PORT A: BYTEWIDE INPUT; 01=PORT A: BYTEWIDE OUTPUT; 10=ENABLE SLAVE PORT; 11=ENABLE
1	0
0	0

PARALLEL PORT B

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	PRIMARY FUNCTION DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPA-BILITY
A5	J2/8	8	PB7	OUT	PARALLEL AND BITWISE I/O		IA5		I/O
A4	J2/7	11	PB6	OUT			IA4		I/O
A3	J2/6	12	PB5	IN			IA3	SA1	I/O
A2	J2/5	13	PB4	IN			IA2	SA0	I/O
A1	J2/4	14	PB3	IN			IA1	/SRD	I/O
A0	J2/3	15	PB2	IN			IA0	/SWR	I/O
RESERVED	na		PB1	IN			CLKA	CLKA	I/O
SPI CLK	J2/2	5	PB0	IN			CLKB	CLKB	I/O

PORT B
DATA DIRECTION REGISTER
PBDDR (0x47)

Bits 7–0: 0 = CORRESPONDING BIT IS INPUT; 1 = CORRESPONDING BIT IS OUTPUT

PARALLEL PORT C

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	PRIMARY FUNCTION DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPA-BILITY
RESERVED	J1/22		PC7	IN		INPUT		RXA	IN
RESERVED	J1/21		PC6	OUT	OUTPUT		TXA		OUT
SPI MI	J1/20	6	PC5	IN		INPUT		RXB	IN
SPI MO	J1/19	7	PC4	OUT	OUTPUT		TXB		OUT
LINK RxC	J1/18	n/c	PC3	IN		INPUT		RXC	IN
LINK TxC	J1/17	n/c	PC2	OUT	OUTPUT		TXC		OUT
RS232 RxD	J1/16	n/c	PC1	IN		INPUT		RXD	IN
RS232 TxD	J1/15	n/c	PC0	OUT	OUTPUT		TXD		OUT

PORT C
FUNCTION REGISTER
PCFR (0x55)

7	0
6	TXA
5	0
4	TXB
3	0
2	TXC
1	0
0	TXD

0 = CORRESPONDING BIT FUNCTIONS NOMALLY AS OUTPUT
1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

LEGEND

- RCM3000 pin either an input or output.
- RCM3000 pin is an input .
- RCM3000 pin is an output.
- All cells non-colored are not used, or they require no programming.

PARALLEL PORT D

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	PRIMARY FUNCTION DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPA-BILITY
LED4	J1/32	n/c	PD7	IN	PARALLEL AND BITWISE I/O			ARXA	I/O
LED3 - f.e. comm	J1/31	n/c	PD6	IN			ATXA		I/O
LED2 - error	J1/28	n/c	PD5	IN				ARXB	I/O
LED1 - heartbeat	J1/27	n/c	PD4	IN			ATXB		I/O
LED7	J1/26	n/c	PD3	IN					I/O
LED8	J1/29	n/c	PD2	IN					I/O
RESERVED	J1/34		PD1	IN					I/O
RESERVED	J1/33		PD0	IN					I/O

PORT D
FUNCTION REGISTER
PDFR (0x65)

7	0
6	ATXA
5	0
4	ATXB
3	0
2	0
1	0
0	0

0 = CORRESPONDING BIT FUNCTIONS NOMALLY AS I/O
1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PORT D
DATA DIRECTION REGISTER
PDDDR (0x57)

Bits 7–0: 0 = CORRESPONDING BIT IS INPUT; 1 = CORRESPONDING BIT IS OUTPUT

PORT D
CONTROL REGISTER
PDCR (0x64)

7	0
6	0
5, 4	TRANSFER CLOCK UPPER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2
3	0
2	0
1, 0	LOWER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2

PORT D
DRIVE CONTROL REGISTER
PDDCR (0x66)

Bits 7–0: 0 = CORRESPONDING BIT AS OUTPUT IS DRIVEN HIGH AND LOW; 1 = CORRESPONDING BIT AS OUTPUT IS OPEN DRAIN

Fig. A.2. RCM port and pin definitions. Full functionality is shown. Refer to the text for those pins used. Columns B and C are the wiring connections between the RCM module and the CPLD.

PARALLEL PORT E

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPA-BILITY
STR7	J2/13	4	PE7	IN	PARALLEL AND BITWISE I/O		I7	/SCS	I/O
STR6	J2/14	3	PE6	IN			I6		I/O
STR5	J2/15	2	PE5	IN			I5	INT1B	I/O
STR4	J2/16	1	PE4	IN			I4	INT0B	I/O
STR3	J2/17	144	PE3	IN			I3		I/O
RESERVED	na		PE2	IN			I2		I/O
INT1	J2/18	143	PE1	IN			I1	INT1A	I/O
INT0	J2/19	142	PE0	IN			I0	INT0A	I/O

PORT E FUNCTION REGISTER PEFR (0x75)

7	I7
6	I6
5	I5
4	I4
3	I3
2	I2
1	I1
0	I0

0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O
1 = CORRESPONDING BIT CARRIES EXTERNAL I/O CONTROL SIGNAL

PORT E DATA DIRECTION REGISTER PEDDR (0x67)

0 = CORRESPONDING BIT IS INPUT
1 = CORRESPONDING BIT IS OUTPUT

PORT E CONTROL REGISTER PECR (0x74)

7	0	TRANSFER CLOCK
6	0	
5–4		UPPER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2
3	0	
2	0	
1–0		LOWER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2

PARALLEL PORT F

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPA-BILITY
CAPT1	J2/12	138	PF7	IN	PARALLEL AND BITWISE I/O		PWM3		I/O
CAPT2	J2/11	139	PF6	IN			PWM2		I/O
misc.	J2/10	140	PF5	IN			PWM1		I/O
misc.	J2/9	141	PF4	IN			PWM0		I/O
LED5	J1/11	n/c	PF3	IN					I/O
LED6	J1/12	n/c	PF2	IN					I/O
	J1/13		PF1	IN			CLKC	CLKC	I/O
INTACK	J1/14	60	PF0	IN			CLKD	CLKD	I/O

PORT F FUNCTION REGISTER PFFR (0x3D)

7	PWM3
6	PWM2
5	PWM1
4	PWM0
3	0
2	0
1	CLKC
0	CLKD

0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O
1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PORT F DATA DIRECTION REGISTER PFDDR (0x3F)

0 = CORRESPONDING BIT IS INPUT
1 = CORRESPONDING BIT IS OUTPUT

PORT F CONTROL REGISTER PFCR (0x3C)

7	0	TRANSFER CLOCK
6	0	
5–4		UPPER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2
3	0	
2	0	
1–0		LOWER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2

PORT D DRIVE CONTROL REGISTER PFDCR (0x3E)

0 = CORRESPONDING BIT AS OUTPUT IS DRIVEN HIGH AND LOW
1 = CORRESPONDING BIT AS OUTPUT IS OPEN DRAIN

PARALLEL PORT G

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPA-BILITY
	J2/20		PG7	IN	PARALLEL AND BITWISE I/O			RXE	I/O
	J2/21		PG6	IN			TXE		I/O
LCD_led5	J2/22	66	PG5	IN			RCLKE	RCLKE	I/O
LCD_led4	J2/23	63	PG4	IN			TCLKE	TCLKE	I/O
	J1/26		PG3	IN				RXF	I/O
	J1/25		PG2	IN			TXF		I/O
	J1/24		PG1	IN			RCLKF	RCLKF	I/O
	J1/23		PG0	IN			TCLDF	TCLKF	I/O

PORT G FUNCTION REGISTER PGFR (0x4D)

7	0
6	TXE
5	RCLKE
4	TCLKE
3	0
2	0
1	RCLKF
0	TCLKF

0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O
1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PORT G DATA DIRECTION REGISTER PGDDR (0x4F)

0 = CORRESPONDING BIT IS INPUT
1 = CORRESPONDING BIT IS OUTPUT

PORT G CONTROL REGISTER PGCR (0x4C)

7	0	TRANSFER CLOCK
6	0	
5–4		UPPER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2
3	0	
2	0	
1–0		LOWER NIBBLE: 00 - PCLK/2; 01 - TIMER_A1; 10 - TIMER_B1; 11 - TIMER_B2

PORT D DRIVE CONTROL REGISTER PGDCR (0x4E)

0 = CORRESPONDING BIT AS OUTPUT IS DRIVEN HIGH AND LOW
1 = CORRESPONDING BIT AS OUTPUT IS OPEN DRAIN

OTHER PIN ASSIGNMENTS

DEFAULT SIGNAL	RCM3000 CONN. / PIN	ALTERA PIN	PIN	DEFAULT	FUNCTION
(LCD_led6)	J2/25	67	/IORD	OUT	Aux. I/O Strobe
(LCD_led7)	J2/24	68	/IOWR	OUT	Aux. I/O Strobe
/RSTout	J2/1	22	/ROUT	OUT	Reset Out
	J2/31		+3.3V		
	J1/1		GND0		
	J2/32		GND1		
	J2/34		GND2		
	J2/30		VBAT		ext. 3.0V battery
	J2/28		/RST_IN		input reset sig.

DATA REGISTERS

PADR	(0x30)
PBDR	(0x40)
PCDR	(0x50)
PDDR	(0x60)
PEDR	(0x70)
PFDR	(0x38)
PGDR	(0x48)

I/O BANK CONTROL REGISTER (addr IBxCR = 08xh)

Bits 7,6	Bits 5,4	Bit 3	Bit 2	Bits 1,0
Wait state code: 11 - 1 Wait states; 10 - 3 Wait States; 01 - 7 Wait States; 00 - 15 Wait states	Strobe type: 00 - Chip select; 01 - Read strobe; 10 - Write strobe; 11 - Read and write	1 - Permit write; 0 - Inhibit write	1 - Active high strobe; 0 - Active low strobe	00 Ignored

EXTERNAL I/O REG. ADDRESS RANGE & PIN MAPPING

Control Register	Port E Pin	I/O Address A[15:13]	I/O Address Range
IB0CR	PE0	000	0x0000-0x1FFF
IB1CR	PE1	001	0x2000-0x3FFF
IB2CR	PE2	010	0x4000-0x5FFF
IB3CR	PE3	011	0x6000-0x7FFF
IB4CR	PE4	100	0x8000-0x9FFF
IB5CR	PE5	101	0xA000-0xBFFF
IB6CR	PE6	110	0xC000-0xDFFF
IB7CR	PE7	111	0xE000-

Fig. A.3. RCM port and pin definitions continued.

APPENDIX SECTION B

This section includes some Rabbit Semiconductor documentation for convenience.

BitWrPortI( ) <SYSIO.LIB>

SYNTAX: void BitWrPortI(int io_port, char *PORTShadow, int value, int bitcode);
KEYWORDS: parallel port
PARAMETER1: address of internal I/O port.
PARAMETER2: address of variable shadowing current value of port.
PARAMETER3: value to write to port.
PARAMETER4: bit (0-7) to write value to.
DESCRIPTION: Updates shadow register at bit with value (0 or 1) and copies shadow to I/O port. WARNING: a shadow register is REQUIRED for this function. All of the Rabbit internal registers have predefined macros corresponding to the register's name. PADR is #defined to be 0x30, etc.
RETURN VALUE: None

WrPortI( ) <SYSIO.LIB>

SYNTAX: void WrPortI(int io_port, char *PORTShadow, int data_value);
KEYWORDS: parallel port
PARAMETER1: address of internal I/O port.
PARAMETER2: address of variable shadowing current value of port.
PARAMETER3: value to write to port.
DESCRIPTION: Writes an internal I/O port with 8 bits and updates shadow for that port. The variable names must be of form "Port" and "PORTShadow" for most efficient operation. A null pointer may be substited (use "NULL") if shadow support is not desired or needed. All of the Rabbit internal registers have predefined macros corresponding to the register's name. PADR is #defined to be 0x30, etc.

NOTE: This function is interruptible and shadow values should not be assumed to be safe if modified in user defined interrupts
RETURN VALUE: none

SetVectExtern3000( ) <SYS.LIB>

SYNTAX: unsigned SetVectExtern3000(int interruptNum, void *isr);
DESCRIPTION: Function to set one of the external interrupt jump table entries for the Rabbit 3000 CPU and some versions of the Rabbit 2000. All Rabbit interrupts use jump vectors. See SetVectIntern for more information.
PARAMETER1: External interrupt number. Two are possible -- 0 and 1 are the only valid values.
PARAMETER2: ISR handler address, ie pointer to a function. Must be a root address.
RETURN VALUE: 0 failed
!=0 NON-RABBITSYS: jump address in vector table
RABBITSYS: isr
SEE ALSO: GetVectExtern3000, SetVectIntern, GetVectIntern

The Utils.lib file includes custom functions:

ExtIOWrite( )

SYNTAX: void ExtIOWrite(word addr, char data);
int ExtIORead(word addr);